

## **REMARKS**

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the Office Action of December 8, 2004 (hereinafter "Office Action"). In response, Applicants confirm the election of Claims 1 - 8, 16 - 23, and 27 - 34. Applicants respectfully submit that the cited reference fails to disclose or suggest all of the recitations of the independent claims. Therefore, Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

### **Double Patenting**

Claims 1, 4, 6, 7, 16, 19, 21, 22, 27, 30, 32, and 33 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1, 3, 31, and 59 of copending Application No. 09/852,562. (Office Action, page 4). Applicants will submit a Terminal Disclaimer in the present case should the cited application issue as a patent.

### **Independent Claims 1, 6, 16, 21, 27, and 32 are Patentable**

Claims 1, 6, 16, 21, 27, and 32 stand rejected under 35 U.S.C. §102(e) as being anticipated by U. S. Patent No. 6,327,647 to Moyer et al. (hereinafter "Moyer"). (Office Action, page 5). Independent Claim 1 is directed to a method of operating a cryptographic data processing system and recites, in part:

...  
loading at least one operand from the system memory to the local memory; and  
executing an instruction using the cryptographic processor that references the at least one operand using a first relative position in the local memory.

Claims 6, 16, 21, 27, and 32 include similar recitations. Thus, according to independent Claim 1, the cryptographic processor executes the instruction such that one or more operands are referenced using a relative position in a local memory, as opposed to, for example, storing the one or more operands in a register. This aspect of the present invention is discussed, for

example, at page 13, lines 15 through 32 of the present application.

In sharp contrast, Moyer describes a data processing system in which operands are passed from a processor 12 to coprocessors 14, 16. (Moyer, col. 8, lines 56 - 67). Moyer appears to contain no discussion, however, about how the coprocessors 14, 16 store the operands for use when executing an instruction. Applicants acknowledge that Moyer describes a coprocessor 14 as having storage circuitry 104 (see Moyer, FIG. 3). Moyer explains, however, that the storage circuitry 104 is optional (Moyer, col. 5, lines 37 - 39) and does not provide any indication with respect to whether operands are stored in a memory, such as the storage circuitry 104, for use by the coprocessor 14 in executing an instruction.


For at least these reasons, the Applicant respectfully submits that Claims 1, 6, 16, 21, 27, and 32 are patentable over the cited reference and that dependent Claims 2 - 6, 7, 8, 17 - 20, 22, 23, 28 - 31, 33, and 34 are patentable for at least the reason that they depend from an allowable claim.

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### CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,




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